

Electronic systems are nowadays the result of the convergence of different technologies. Therefore a combination of experience, techniques, tools and a proper contact network is mandatory to meet market expectations. By working with **YOGITECH**, customers leverage on the company's solid partnership with top-tier EDA tool vendors. Years of experience dealing with world-wide customers and a proven track of right-first-time designs make **YOGITECH** reliable for any kind of IC design.

Projects at **YOGITECH** are managed by specifications, timescale and budget, previously agreed with clients. This disciplined yet flexible approach combines with **YOGITECH**'s methodology, skills and know-how, delivering customer satisfaction and business renewal. **YOGITECH** is actively involved in SoCs or ASICs design & verification, including implementation or re-use of IP blocks (digital, analogue and verification), providing point solutions and filling resource shortfalls.

# System-on-Chip

**Systems-on-Chip (SoC) are one of the biggest challenges engineers ever faced.**

**They are the result of a mix of microprocessors, memories, busses, architectures, communication standards, protocol processors, interfaces and other intellectual property components where system level considerations such as power optimization, synchronisation, testability, conformance and verification are crucial.**

**Yogitech's outstanding experience with CPUs (e.g. ARM) interconnect standards (such as OCP or AMBA/AXI) and protocols (such as ATAPI, CAN, LIN and PCI) make it easier to match all system requirements.**

**Yogitech's approach always begins with a fully detailed verification plan and it is based on a strong interaction between digital and analogue expertises and the use of the most advanced verification techniques.**

**Yogitech's involvement into a project can span from specs to tape out (all intermediate steps included), working independently or in team with the customer. Yogitech's expertise includes design of customized IPs providing highest-quality deliverables such as datasheets, characterization layout constraints, coverage reports, implementation, verification scripts, etc.**

**Yogitech's design track record includes projects for the global worldwide leaders SIPs and OEMs in the automotive, biomedical and telecom sector.**

## S U C C E S S S T O R I E S

- \_ ARM7-based SoC for automotive applications with optimized architecture for testability and minimum IOs count.
- \_ 8051-based ASIC with peripherals for automotive and aerospace applications, including FPGA pre-silicon prototyping.
- \_ Mixed-signal SoC with CPU and LIN/SPI interfaces.
- \_ ARM9-based SoC for ADSL modems with custom high-speed peripherals.
- \_ 5MGates ASIC for SDH/ATM switches with LVDS and PCI interfaces.
- \_ Custom IP for sensor data processing including ARC processors.
- \_ Design of BIST blocks for embedded memories.

## E X P E R T I S E S

- \_ ARM. ARM7, ARM9 and ARM11 cores.
- \_ Other cores. 8051, 80515, ARC, x86
- \_ Interconnects. AMBA, AXI, OCP, STBUS.
- \_ Automotive. CAN, LIN, SPI, FlexRay, I2C.
- \_ Telecom/comm. PCI, PCI EXPRESS, ATM, SDH, SONET, Ethernet, UART.
- \_ Data Storage/Multimedia. ATAPI, HDMI, USB, MPEG.

# System-on-Chip

## ARM and CPU-based Architectures

Yogitech, member of the ATAP partnership, has a long track record on ARM system such as system architecture and partitioning, system verification and debug at board level, design of AHB/APB/AXI devices, use of ARM's PrimeCells, front-to-back and back-end support, use of ARM RVDS developer suite, MultilICE, ARM Emulator boards, development of ARM-based firmware. Yogitech brought many ARM projects to the tape out, such as ARM7-based systems for automotive applications and ARM9-based SoC for ADSL modems. Yogitech's expertise in CPU-based architectures includes 8051, 80515, ARC, DSPs emulation boards of off-the-shelf MCUs such as NEC, Freescale, and others.

## Testability, Reliability and Fault Robustness

Yogitech's SoC design team has a distinguishing competency in Design-for-Robustness and a deep knowledge of Testability and Reliability issues, of standard requirements such as IEC 61508, a consolidated experience in BIST, BISR, IEEE 1149.1 design and a well defined design flow including FMEA most advanced DFT techniques and tools.

## SoC Design flow

Yogitech's SoC flow supports both Verilog, VHDL, SystemC and SystemVerilog descriptions starting from system specification and partitioning until the tape-out, passing from RTL Design and Verification (Static and Dynamic), synthesis techniques for low-power or very high-speed applications, Physically aware synthesis, Static Timing Analysis, Formal Verification, fast prototyping with FPGA, Test Insertion and ATPG, Advanced Place&Route with IPO and signal integrity. Testability, Reliability analysis and Functional Verification are applied during the entire flow. The design flow takes into account the use of EDA tools from leading providers such as Cadence, Mentor and Synopsys. Yogitech's stories include SoC taped-out with technologies from 0.13µm to 0.35µm, and experiences in the ultradeep sub micron range such as 0.09

## Business Model

Different business models are available. Time & Material for services to be carried out either on customer site or in house. Per task, based on a detailed Statement of Work defined with the customer. On selected projects Yogitech can provide a full turnkey service including foundry, assembly and testing management.

*Yogitech reserves the rights to make any changes in this document and related service in any time without prior notice. No responsibility is accepted for errors or omissions.*

