

Electronic systems are nowadays the result of the convergence of different technologies. Therefore a combination of experience, techniques, tools and a proper contact network is mandatory to meet market expectations. By working with **YOGITECH**, customers leverage on the company's solid partnership with top-tier EDA tool vendors. Years of experience dealing with world-wide customers and a proven track of right-first-time designs make **YOGITECH** reliable for any kind of IC design.

Projects at **YOGITECH** are managed by specifications, timescale and budget, previously agreed with clients. This disciplined yet flexible approach combines with **YOGITECH**'s methodology, skills and know-how, delivering customer satisfaction and business renewal. **YOGITECH** is actively involved in SoCs or ASICs design & verification, including implementation or re-use of IP blocks (digital, analogue and verification), providing point solutions and filling resource shortfalls.

Verification

Recent statistics show that 60-70% of the entire product cycle for a complex logic chip is dedicated to verification tasks: 71% of SoC re-spins are due to logic bugs, and 47% of them are due to incorrect or incomplete specifications. Moreover, 14% of failing SoCs have bugs in reused components or IPs. Traditional verification methodologies (direct testing) have been proven to be inadequate to recognize all bugs because of the multiple possible verification cases. Therefore, verification efforts increase exponentially with the complexity of systems and with the design size.

Yogitech's verification team can solve any system or module level verification problem thanks to its consolidated and worldwide recognized experience in the use of random constraint-driven and coverage-driven methodology based on Cadence's VPA solutions. A detailed list of checks and coverage items is implemented after a sharp definition of the verification plan, and tests are generated making it possible to bring forth hard-to-reach corner cases. In this task Yogitech integrates other cutting-edge methodologies, such as static or pseudo-static functional verification or co-verification with SW or SystemC. In addition to its own verification IPs, Yogitech can be commissioned to design dedicated eVCs to match specific customer requirements.

S U C C E S S S T O R I E S

- _ Validation and system level verification of Ethernet over Sonet/SDH IP.
- _ Functional validation of a Display subsystem for wireless platform.
- _ Functional verification of an OCP to Customer Protocol Bridge.
- _ OCP interfaces validation of a 3D Graphics subsystem.
- _ Verification of a SRAM-ROM memory controller with the AXI protocol.
- _ Development of monitors, protocol checker, coverage items and scoreboard with regression support for a configurable DDR/DDR2 Controller.
- _ System level verification using C driven testbenches, VHDL stubs modelling and Silicon validation for a Dual ARM based chip.

E X P E R T I S E S

- _ Verification of ARM's architectures.
- _ Verification of 8051-based architectures.
- _ Interconnects. AMBA, AXI, OCP, STBUS, DTML.
- _ Automotive. CAN, LIN, SPI, FlexRay, I2C.
- _ Telecom/comm. PCI, PCI EXPRESS, ATM, SDH, SONET, Ethernet, UART.
- _ Data Storage/Multimedia. ATAPI, HDMI, USB, MPEG.



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Verification

Module level verification

Yogitech's track record of success stories in module verification covers most of the bus architectures and protocols. Module level verification environment is usually built around re-usable and eRM compliant verification IPs.

System level verification

Yogitech has the experience in SoC design to challenge and overwhelm the problems of complex verification environments where subsystems with multiple ports and protocols should be verified taking into account the running application. Yogitech's methodology can be used to build verification environments in which individual IP verification cooperates with top-level sequence drivers, interacting with SW application through the use of advanced CoVerification Links. Yogitech's distinguishing experience is the verification of ARM-based and 8051-based SoCs.

Mixed-Language and Mixed-Signal verification

Yogitech can combine different verification approaches: standard, static, dynamic, formal and others. In addition, Yogitech developed its own methodology for mixed-signal verification which combines digital verification and analogue modelling, a top-level approach to control checks coverage for mixed analogue-digital system.

Verification flow

Yogitech's verification flow is mainly based on Cadence's VPA solutions (Specman Elite, eAnalyzer, vManager, SpeXSim, SpeXtreme). It also includes different methodologies (static and formal verification, PSL, SystemVerilog, SystemC modelling) and standard approaches (VHDL or Verilog testbenches). Yogitech's Verification flow includes System Specification analysis, verification plan development, Detailed Block level verification plan, Block level verification development (reusable), System level verification, Coverage report and Functional verification report.

Business model

Different business models are available. Time & Material for services to be carried out either on customer site or in house. Per task, based on a detailed Statement of Work defined with the customer. On selected projects Yogitech can provide a full turnkey service including foundry, assembly and testing management.

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