Company and Products Overview

YOGITECH

The One Stop Shop for Functional Safety
YOGITECH milestones

2000
YOGITECH incorporated

2001
Joining ARM Technology Alliance Partnership and Verisity Verification Alliance

2003
OCP, CAN and ATAPI Verification Components introduced in the market

2005
First round funding by Toscana Ventures

2006
faultRobust launched in the market

2007
fRCPU, first IEC61508 SIL3 compliant IP launched in the market

2008
Verification assets sold to Cadence

2011
Second round funding by Atlante Ventures

2012
First lead customers of fRTools

2014
fRSTL certified

2015
QMS certified

Currently 46 people
Headquarter in Pisa (Italy)
office in Milan (Italy)
Branch in Japan (YOGITECH KK)

Customers:
most of IP, IC and FPGA providers;
major Tier2, Tier1 and OEM worldwide.
Strong focus on ADAS
YOGITECH business lines

fRTools
EDA tools enabling customers to independently perform safety analysis and verification

fRMetho\'dology
Functional safety analysis and verification

fRSTL
Software Test Libraries implementing safety mechanisms

fRIPs
Hardware IPs implementing safety mechanisms

The one stop shop for Functional Safety
Business strategy overview

Consolidation of the position in Japan by reinforcing business development, local support and partnerships through Yogitech KK

Investment in new geographical areas (i.e. US and Germany) based on the experience in Japan

2014 Revenue

Area
- 24% JP
- 41% US
- 34% EU

Customers
- 2% IP
- 69% SIP
- 29% Tier1/OEM

Market
- 75% Auto.
- 24% Indus.
- 1% Other

Scaling up the value chain from IDM to Tier1 and OEM; extending to IP provider for a full consistent value chain

Consolidation of the market share into the Automotive sector and expansion into different market application with emphasis on the Industrial domain. Attacking security area in the medium term
YOGITECH key role in safety

• YOGITECH is driving the application of functional safety standards to integrated circuits, by actively participating to *international working groups* and *committees* and contributing to the preparation of international normative

**ISO 26262**
- Expert member of ISO 26262 WG
- Leader of ISO 26262-10 Annex A about how to apply ISO 26262 to microcontrollers
- Co-leader of ISO/PAS 19451 (ISO 26262 semiconductor group)
- Leader of new ISO 26262-11, including all semiconductor contents

**IEC 61508**
- Participating to soft-errors definition in IEC 61508 2nd edition
YOGITECH: The One Stop Shop for functional Safety

We support our customers for all their safety matters:

**KNOWLEDGE**

**fRTtrainings**
Specific on-site trainings on ISO26262 and IEC61508 applied to ICs based on experience in different application domains

**DESIGN**

**fRMmethodology**
A patented white-box approach to perform functional safety assessment and safety-oriented design exploration of ICs according IEC 61508 and ISO 26262
- Functional safety assessment of integrated circuits (including review of the design process)
- Fault injection
- Specification (and if required also development) of safety mechanisms for custom HW or SW IPs

**fRTtools**
A collection of licensable tool suites that allows the user to independently perform FMEDA and safety verification of integrated circuits according to the requirements of IEC 61508 and ISO 26262

**INTEGRATION**

**fRIPs (faultRobust IPs)**
HW IPs implementing safety mechanisms for basic modules of an IC like CPU, MEM, BUS and Peripherals

**fRSTL (faultRobust SW Test Libraries)**
SW units implementing safety mechanisms for basic modules of an IC like CPU, MEM, BUS and Peripherals

**Business Model**

**Consultancy and EDA licensing**

**IP licensing + royalties**

YOGITECH S.P.A. - Proprietary
YOGITECH organizes at customer site dedicated trainings on **ISO 26262** and **IEC 61508**, with focus on how to apply those functional safety standards to integrated circuits (MCU, ASIC, sensors and FPGA) and system level.

A training is typically organized in 2 or 3 days:

- One day describing ISO 26262 / IEC 61508 in general
- One or two days about how to specify, design, implement and verify an integrated circuit or ECU according ISO 26262 / IEC 61508
- It includes practical examples on different safety architectures
- One “hands-on” day focused on a case study

All Training courses can be customized based on customer’s needs
fRMethodology

- To perform functional safety analyses and safety-oriented design exploration of integrated circuits (SoC, MCU, ASIC, FPGA) and systems according to ISO 26262 and IEC 61508

The complexity of modern integrated circuits is such that the traditional black-box approach is no longer realistic.

Patented white-box approach looking inside an integrated circuit to ensure as much safety as needed.

- It consists of:
  - **dividing** the component into Elementary Parts (EP) by using automatic tools to guarantee the completeness of the analysis;
  - **computing** the ISO 26262 safety metrics by looking to the fault models of each elementary part, attributing the failure rate and estimating the diagnostic coverage of the planned HW or SW safety mechanisms;
  - **verifying** the safety metrics by an extensive fault injection campaign simulating permanent, transient and common cause faults.
Key ISO 26262 requirements covered by fRMethodology

- Review of Functional Safety Management / Process Safety Audit (ISO 26262-2 and -10)
- Definition of assumed safety requirements with respect to Functional (ISO 26262-3) and Technical (ISO 26262-4) safety concepts
- Specification / review of HW safety requirements, HW design and HW-SW interface (ISO 26262-5)
- Computation of the failure rates, preparation / review of FMEA, DFMEA, FMEDA, FTA (ISO 26262-5, -10)
- Evaluation of HW architectural metrics and safety goal violations due to random HW failures, including providing suggestions & solutions about how to cover the gaps, if any (ISO 26262-5, -10)
- Preparation / review of Verification and Validation plan (ISO 26262-4, -5, -8)
- Verification and validation of effectiveness of safety mechanisms, including fault injection (ISO 26262-4 and ISO 26262-5)
- Specification / review of SW safety requirements with respect to FW and SW units (ISO 26262-6)
- Review of SW tools confidence in use (ISO 26262-8)
- Review of ASIL decomposition, FFI and DFA analyses (ISO 26262-9)
- Review of degree of fulfilment of IC specific recommendations, IC Safety Manual (ISO 26262-10)
The **fRTools** are a collection of licensable tool suites that allows the user to independently perform FMEDA and safety verification of integrated circuits according to the requirements of IEC 61508 and ISO 26262.

With the fRTools YOGITECH’s customers can run the safety analysis and verification of their designs, in their own design environment, maintaining the full control of their intellectual property, while still being sure to have gone through all the steps included in the fRMethodology coherently to the target safety standards.

**fRTools portfolio includes:**

- **Safety Designer tool suite**
- **Safety Verifier tool suite**
Safety Designer Tool Suite

- It automates the safety analysis of integrated circuits according to safety standards like ISO 26262 and IEC 61508.

- It allows the user to analyze the integrated circuit at different levels of abstraction, to partition it into its elementary parts, to associate the failure modes to functional blocks and elementary parts, to compute the safety metrics and to estimate the safeness and diagnostic coverage.

- **Main features**
  - Computing failure rates
  - Determining failure modes and associating them with the IC database to compute failure modes distribution
  - Doing safety analyses like FMEDA, FTA and DFA
  - Comparing estimations with fault injection results
  - Preparing Safety Verific. Plan
Safety Verifier Tool Suite

- It automates the verification of safety metrics (safeness and diagnostic coverage of HW and SW mechanisms) by managing fault injection campaigns on integrated circuits.
- It allows the user to partition the campaign according to the Safety Verification Plan defined in Safety Designer.
- It manages all the necessary simulations (run by an external fault or functional simulator, depending on the fault model) and integrates the results into a comprehensive view for the portions of hardware injected.

Main features
- Importing Safety Verification Plan from Safety Designer
- Preparing the fault injection setup including generating the fault lists from IC database, generating vectors for black-box macros etc…
- Injecting permanent, transient and special (e.g. shorts, clock, reset) faults
fRIPs and fRSTL

**fRIPs**

- HW modules implementing safety mechanisms for basic units like CPU, MEM, BUS and Peripherals, aimed to reach appropriate Safety Integrity Level at IC level

- Can detect faults at real time, allow continuous operation

**fRSTL**

- SW modules implementing safety mechanisms for basic units like CPU, MEM, BUS and Peripherals, aimed to reach appropriate Safety Integrity Level at IC level

- Can detect faults only when invoked. Test is executed on an infrequent basis depending on the safety concept implemented
fRIPs

- **fRCPUs**
  - Optimized tightly coupled fault supervisor for low-cost safety concepts
  - Included in ISO 26262 as “asymmetric redundancy” (ISO 26262-5 D.2.3.6)

- **fRSmartComp**
  - Enhanced dual-core lock-step for high safety fail operational safety concepts
  - Included in ISO 26262 as “2-way voting” (ISO 19451 PAS D.2.3.10.2)

- **fRMEM**
  - Provides error correction codes (ECC) for RAM, DRAM, ROM or FLASH
  - Includes scrub&repair and local memory protection unit

- **fRBUS**
  - Supervises multilayer bus as AHB AMBA
  - Composed by a set of scoreboards plus a central supervisor

- **fRNET**
  - Collects all the alarms and failures information generated by fRIPs
  - It provides different format for error signal outputs

**Optimized die-size, architectural + functional diversity, latent faults detection, detailed diagnostic information, fail operational and availability**
Diagnostic SW Test libraries for detecting HW random faults, developed using an fRMethology based whitebox approach

Each TS:
- targets a specific function or a group of functions of the component
- provides pass/fail information and self-checking signatures (CRC)
- may be interrupted at any time by the application SW
# fRSTL_stm32 portfolio

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<thead>
<tr>
<th>STM32</th>
<th>Cortex-M0</th>
<th>Cortex-M3</th>
<th>Cortex-M4</th>
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fRSTL_xmc portfolio
fRSTL_arm portfolio

Addressing the complete ARM CM family: CM0, CM0+, CM3, CM4.

Extension to Cortex-A family under development
Thank you!

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